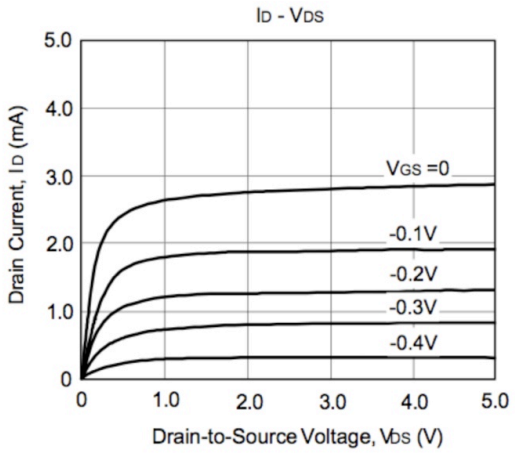
EECS 2077 Test #3, Fall 2016 Name:_____

#1 ____/25 pts
#2 ____/28 pts
#3 ____/22 pts
#4 ____/24 pts

Allowed materials: 3 pages of 1-sided equation sheets, writing utensil, calculator.
Remember – we use cgs units! Centimeter/gram/second.

kT = 0.026 eV (300K) ε_0=8.854x10^{-14} F/cm ε_r(Si)=11.8 ε_r(SiO_2)=4.0
q= 1.6x10^{-19} C n_i(Si)=1.5x10^{10} / cm^3

1.) [25 pts.] Let's begin with some review and play the drift versus diffusion game! Circle the correct answer for each:



a) Determines the current required at the gate of the JFET plot (shown at right) for the case of V_{GS} = -0.3V. [5 pts.]

DRIFT DIFFUSION BOTH ARE THE SAME MAGNITUDE BOTH ARE ZERO

b) Determines the current required at the gate of the JFET plot for the case of V_{GS} = +0.3V. [5 pts.]

DRIFT DIFFUSION BOTH ARE THE SAME MAGNITUDE BOTH ARE ZERO

c) Is the main current type across a Schottky (metal-semidonductor) junction with 0V applied . [5 pts.]

DRIFT DIFFUSION BOTH ARE THE SAME MAGNITUDE BOTH ARE ZERO

d) Is the main current type from drain to source in a MOSFET that is above threshold. [5 pts.]

DRIFT DIFFUSION BOTH ARE THE SAME MAGNITUDE BOTH ARE ZERO

e) Is the main current type from the emitter to the base in a BJT in normal forward active mode [5 pts.]

DRIFT DIFFUSION BOTH ARE THE SAME MAGNITUDE BOTH ARE ZERO

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2) [28 pts] Question related to an p-MOS transistor with the following parameters:

The gate electrode 'metal' is n+ poly Silicon.

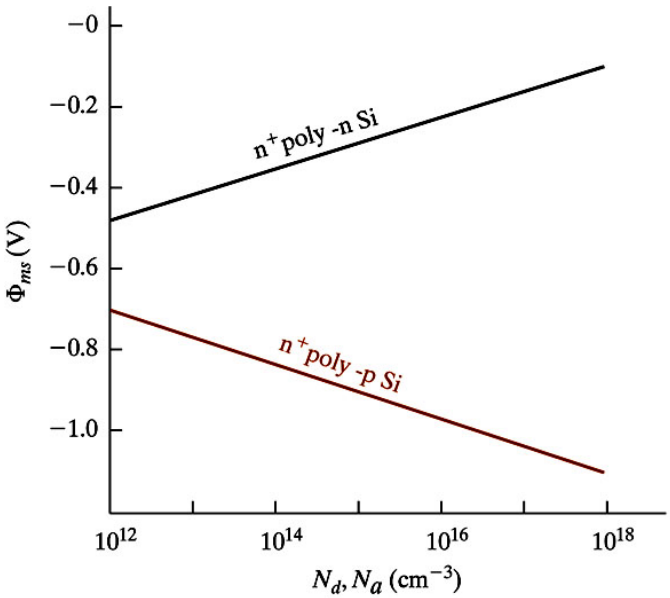
The substrate is doped with Phosphorus to the level of $N_a=10^{15}/cm^3$.

In the plot shown at right, the curves are labeled as 'gate material – substrate material'.

The gate oxide is has a thickness of 10 nm and a dielectric constant of 3.9.

There is no interface charge.

$$V_T = \phi_{ms} - \frac{Q_i}{C_i} - \frac{Q_{D,\max}}{C_i} + 2\phi_f$$



a) right off the bat, tell me the effect of the last two terms ($-Q_i/C_i$), ($2\phi_f$) on threshold voltage magnitude:

THEY INCREASE IT THEY DECREASE IT ONE INCREASES, ONE DECREASES

b) at threshold voltage, calculate by how much will semiconductor bands need to be bent right underneath the oxide surface [5 pts]:

c) provide the value for how much threshold voltage is influenced by the fact that the Fermi level of the gate electrode and the Fermi level of the substrate Si, have to shift to match up at equilibrium [5 pts]:

d) calculate the threshold voltage for this device [13 pts]:

e) at 1 V above threshold voltage, calculate the width of the depletion region [5 pts]:

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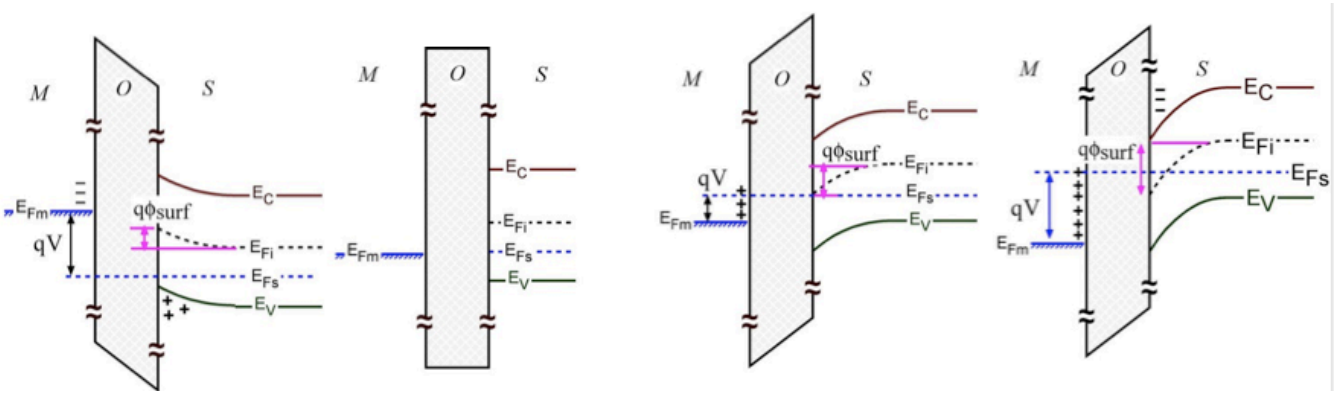
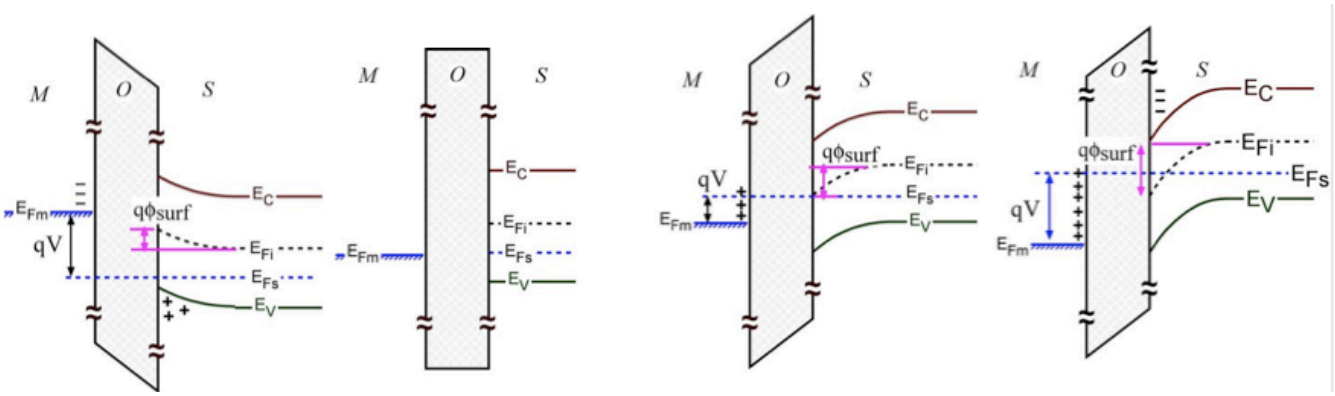
3) [22 pts] Mish-mash of questions…

a) [8 pts] For the diagrams below, draw an arrow in the direction of the E-field, and the length of the arrow should start and end where the E-field starts and ends.



b) [5 pts] For the diagrams below, circle which states give the <u>minimum</u> electrical impedance at the gate. If there are two or more states that are equal in the amount of maxim impedance, circle them.



c) [5 pts] Which has the <u>lowest</u> input impedance for DC voltage signals? Circle one:

MOSFET BJT BOTH ARE SAME, NEITHER

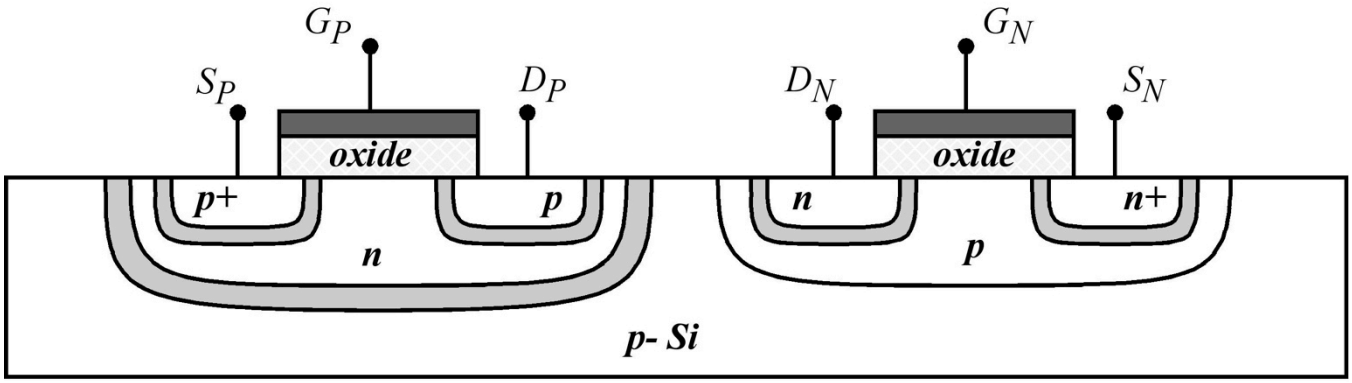
d) [4 pts] Which has the <u>highest</u> impedance for AC voltage signals? Circle one:

DIODE WITH NO VOLTAGE FORWARD BIASED DIODE REVERSE BIASED DIODE

4.) [24 pts] The following is for an ideal pair of NMOS and PMOS devices that form the basis for a logic inverter with threshold voltages that require a change of only 5 V. Perform the following. QUALITATIVE ANSWERS / NO EQUATIONS CALCULATIONS ARE NEEDED.

(a) FIRST: draw an input voltage (V_{IN}) that connects to both gates (G), draw an output voltage (V_{OUT}) that connects to both drains (D), draw a ground on the NMOS source and +5V on the PMOS source.

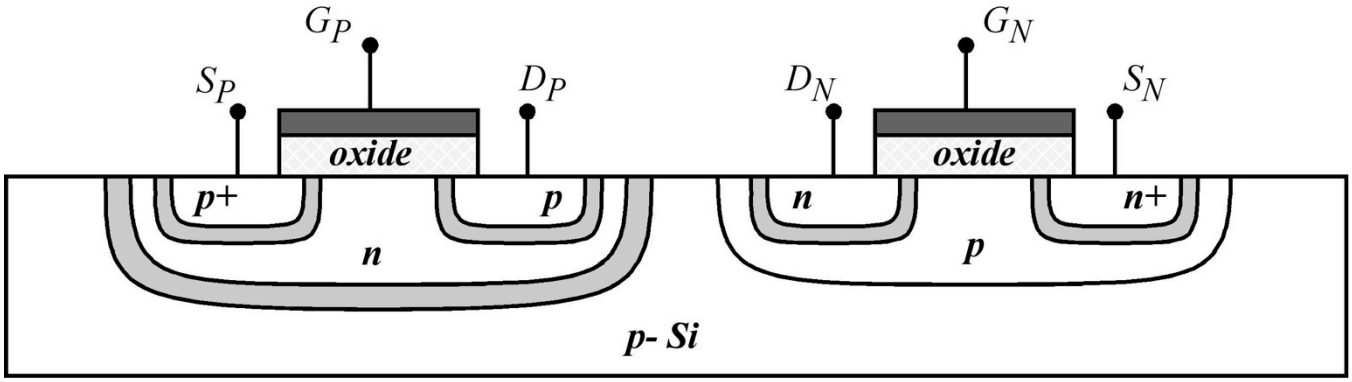
SECOND: using lines with arrows, or directly on the diagram, label as many voltages as possible on each semiconductor region (there are 7 different regions below, 2 points each) for the case of 5V applied to V_{IN}, and also label the voltage at V_{OUT} (just label the voltages at 0V, or 5V, and don't worry about labeling the voltages close to the gate oxide).



(b) Now, lets mix it up a bit…

FIRST: draw an input voltage (V_{IN}) that connects to both gates (G), draw an output voltage (V_{OUT}) that connects to both drains (D), draw 5V on the NMOS source and 10V on the PMOS source.

SECOND: label the diagram similar to how you did for part (a), but do it for the case where the output voltage is 10 V. Note, now you have to label the input voltage too! 1 point each region. You may only label it with voltages such as 10V, 5 V, 0V, 5V, 10V. Do not use any more voltage than is needed to exceed Vth.



EXTRA SPACE